ABSTRACT

Master circuit 1 and slave circuit 2 are designed so that the transistors constituting data-hold differential pairs are smaller in size than the transistors constituting data reading differential pairs. Further, the flip-flop circuit is adapted to operate in an operating speed range in which the currents through the data-hold differential pairs are lower than the currents through the data reading differential pairs, and the currents through the data-hold differential pairs are equal to or lower than the permissible current level of the transistors that constitute the data-hold differential pairs.